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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,136	06/20/2003	Makoto Kudo	81751.0062	5957

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EXAMINER	
LAI, VINCENT	
ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/601,136	KUDO, MAKOTO	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-14 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,2,4-14 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
1/5/2007

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy of the priority documents have been received.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on October 12, 2004 was considered by the examiner.

Response to Amendment

3. Acknowledgement is made of the amendments to the title, claims and abstract.

4. Objections to abstract and title are withdrawn after considering amendments.

Response to Arguments

5. Applicant's arguments filed 2006 December 12 have been fully considered but they are not persuasive.

Applicant argues that the combination of Narayan and Zuraski does not disclose or suggest the features of amended claim 1.

Applicant and Examiner appear to disagree as how the combination of the references is to be applied to the claims of the Specification. Applicant appears to have believed Examiner had intended Zuraski to teach the amended portion of claim 1, whereas Examiner had intended to combine Narayan with Zuraski to teach the amended portion of claim 1. Specifically, Zuraski teaches a shift prefix, which Narayan does not. If Narayan were combined with a shift prefix, the combination would be able to teach the amended portion of claim 1, as Narayan is able to perform the actions of the claims, if the actions did not depend on a shift prefix. Zuraski was cited to show that a shift prefix was known in the art and one having ordinary skill in the art would have been able to take the concept of a shift prefix and apply it to Narayan in such a way that the claims are taught by the combination.

It is noted that the arguments do not pertain to claims 5, 8, 11, 14,17 and 20-22 as the argued limitations pertain to amended claim 1 and the claims listed above do not depend on claim 1.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 9 is dependent on cancelled claim 3 and it is unclear as

to which claim it should now be dependent on. For the purposes of examination, it is assumed to be dependent on claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 5-9, 11-14, and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narayan et al (U.S. Patent # 5,822,559), herein referred to as Narayan, in view of Zuraski, Jr. et al (U.S. Patent # 6,260,134 B1), herein referred to as Zuraski.

As per **claim 1**, Narayan teaches a data processing device which performs pipeline control, the data processing device comprising:

a fetch circuit (Figure element 202, and column 5, lines 38-40) which fetches instruction codes of a plurality of instructions in instruction queues (Column 5, lines 26-28: Queues can be used as a form of a cache), the instructions including a given target instruction (Column 5, lines 63-64: The x86 instructions are the target instructions) and a prefix instruction (Column 16, lines 9-11) which precedes the target instruction and modifies a function of the target instruction (Column 1, line 65- column 2, line 1);

a prefix instruction decoder circuit which performs decode processing only on a prefix instruction (Figure element 207, and column 6, lines 47-49), the prefix instruction decoder circuit receiving the instruction codes of the instructions before decoding that are fetched in the instruction queues (Column 23, lines 6-9: Circuit is pipelined and cannot skip stages), judging whether or not each of the instruction codes is a given prefix instruction (Column 6, lines 59-61: This happens with a Double Dispatch Instruction), and causing a target instruction modifying information register to store information necessary for decoding the target instruction modified by the prefix instruction when the judged instruction code is the given prefix instruction (Column 6, line 61- column 7, line 2); and

a general-purpose decoder circuit which receives each of the instruction codes of the instructions fetched in the instruction queues other than the prefix instruction as a decode instruction, and decodes the decode instruction (Figure element 208, column 6, lines 19-22),

wherein, when the decode instruction is the target instruction, the decoder circuit decodes the target instruction modified by the prefix instruction based on target instruction modifying information stored in the target instruction modifying information register (Column 6, lines 59-61); and

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store information necessary for the target instruction modified by the execution control prefix instruction (Column 18,

lines 48-62), and wherein the decoder circuit decodes the decode instruction based on the information stored in the target instruction modifying information register (Column 18, lines 48-62).

Narayan does not teach wherein the given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction.

Zuraski teaches the use of a shift prefix instruction that is predecoded (or decoded before the main decoder) in order to simplify circuitry (Column 13, line 65-column 14, line 1).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Narayan et al to include a shift prefix instruction to the set of existing prefix instructions. It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Narayan by the teaching of Zuraski because including a shift prefix instruction to the set of existing prefix instructions would simplify the circuitry, thus allowing more space for other units on the device or cutting down on places for errors to occur.

As per **claim 2**, Narayan et al discloses wherein the given prefix instruction

includes an immediate-data expansion prefix instruction for expanding immediate data necessary for execution of the target instruction, function of which is expanded by the prefix instruction (Column 16, lines 30-32),

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store immediate-data expansion information necessary for expanding the immediate data during execution of the target instruction modified by the immediate-data expansion prefix instruction when the input instruction code is the immediate-data expansion prefix instruction (Column 20, lines 61-65: Information is stored in latches), and

wherein the decoder circuit decodes the decode instruction so that the immediate data is expanded at the time of execution of the target instruction that has been modified by the immediate-data expansion prefix instruction based on the immediate-data expansion information stored in the target instruction modifying information register when the decode instruction is the target instruction of the immediate-data expansion prefix instruction (Column 20, lines 53-55).

Claim 3 has been cancelled.

As per **claim 5**, Narayan discloses a data processing device which performs pipeline control, the data processing device comprising:

a fetch circuit (Figure element 202, and column 5, lines 38-40) which fetches instruction codes of a plurality of instructions in instruction queues (Column 5, lines 26-28: Queues can be used as a form of a cache), the instructions including a given target instruction (Column 5, lines 63-64: The x86 instructions are the target instructions) and a prefix instruction (Column 16, lines 9-11) which precedes the target instruction and modifies a function of the target instruction (Column 1, line 65- column 2, line 1);

a prefix instruction decoder circuit which performs decode processing only on a prefix instruction (Figure element 207, and column 6, lines 47-49), the prefix instruction decoder circuit receiving the instruction codes of the instructions before decoding that are fetched in the instruction queues (Column 23, lines 6-9: Circuit is pipelined and cannot skip stages), judging whether or not each of the instruction codes is a given prefix instruction (Column 6, lines 59-61: This happens with a Double Dispatch Instruction), and causing a target instruction modifying information register to store information necessary for decoding the target instruction modified by the prefix instruction when the judged instruction code is the given prefix instruction (Column 6, line 61- column 7, line 2); and

a general-purpose decoder circuit which receives each of the instruction codes of the instructions fetched in the instruction queues other than the prefix instruction as a decode instruction, and decodes the decode instruction (Figure element 208, column 6, lines 19-22),

wherein, when the decode instruction is the target instruction, the decoder circuit decodes the target instruction modified by the prefix instruction based on target instruction modifying information stored in the target instruction modifying information register (Column 6, lines 59-61);

wherein the given prefix instruction includes an execution control prefix instruction for controlling whether or not to execute the target instruction, function of which is expanded by the prefix instruction (Column 18, lines 48-62: This is done with jumps and branches),

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store execution control information necessary for controlling whether or not to execute the target instruction modified by the execution control prefix instruction when the input instruction code is the execution control prefix instruction (Column 18, lines 48-62), and

wherein the decoder circuit decodes the decode instruction so that the target instruction modified by the execution control prefix instruction is executed by judging whether or not to execute the target instruction based on the execution control information stored in the target instruction modifying information register when the decode instruction is the target instruction of the execution control prefix instruction (Column 18, lines 48-62).

As per **claim 6**, Narayan discloses wherein the fetch circuit is connected with

a bus having a width at least twice the width of the instruction code, and fetches the instructions in the instruction queues through the bus in one clock cycle (Column 5, lines 40-42: Instructions are normally 32-bits and the bus is 64-bits).

As per **claim 7**, Narayan discloses wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction (Column 6, lines 6-9), and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction (Figure 2, and column 23, lines 6-9: The device is pipelined).

As per **claim 8**, Narayan discloses wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction (Column 6, lines 6-9), and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction (Figure 2, and column 23, lines 6-9).

As per **claim 9** and in light of above rejection of claim 3, it is rejected based upon similar reasoning as the rejections of claims 7 and 8.

As per **claim 11**, Narayan discloses wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction (Column 6, lines 6-9), and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction (Figure 2, and column 23, lines 6-9).

As per **claim 12**, Narayan discloses wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction (Column 6, lines 6-9), and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction (Figure 2, and column 23, lines 6-9).

As per **claim 13**, Narayan discloses electronic equipment comprising:

the data processing device as defined in claim 1 (Column 209, lines 1-3: The computer system);

means which receives input information (Column 209, lines 1-3: The input from the I/O bus and devices); and

means which outputs a result processed by the data processing device based on the input information (Column 209, lines 1-3: The output from the I/O bus and devices).

As per **claim 14**, Narayan discloses electronic equipment comprising:

the data processing device as defined in claim 2 (Column 209, lines 1-3);

means which receives input information (Column 209, lines 1-3); and

means which outputs a result processed by the data processing device based on the input information (Column 209, lines 1-3).

Claim 15 has been cancelled.

As per **claim 17**, Narayan discloses electronic equipment comprising:

the data processing device as defined in claim 5 (Column 209, lines 1-3);

means which receives input information (Column 209, lines 1-3); and

means which outputs a result processed by the data processing device based on the input information (Column 209, lines 1-3).

As per **claim 18**, Narayan discloses electronic equipment comprising:

the data processing device as defined in claim 6 (Column 209, lines 1-3);

means which receives input information (Column 209, lines 1-3); and

means which outputs a result processed by the data processing device based on the input information (Column 209, lines 1-3).

As per **claim 19**, Narayan discloses electronic equipment comprising:

the data processing device as defined in claim 7 (Column 209, lines 1-3);

means which receives input information (Column 209, lines 1-3); and

means which outputs a result processed by the data processing device based on the input information (Column 209, lines 1-3).

Claims 20-22 are rejected for reasons similar to the rejection of claims 2, 4, and 6, respectively. Claims 20-22 appear to recite the exact same limitations as that of claims 2, 4, and 6, respectively.

8. Claims 4, 10, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narayan in view of Rozenshein et al (U.S. Patent Application Publication # US 2002/0056035 A1), herein referred to as Rozenshein.

As per **claim 4**, Narayan teaches the use of prefix instructions (Column 16, lines 9-12) wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store information necessary for the target instruction modified by the execution control prefix instruction (Column 18, lines 48-62), and

wherein the decoder circuit decodes the decode instruction based on the information stored in the target instruction modifying information register (Column 18, lines 48-62).

Narayan does not teach wherein the given prefix instruction includes a register expansion prefix instruction for expanding a register necessary for execution of the target instruction, function of which is expanded by the prefix instruction.

Rozenshein teaches by the use of a register expansion prefix instruction (Column 5, sections [0070] and [0082]) in order to modify the target instruction if necessary (Abstract).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Narayan et al to include register expansions to set of existing prefix instructions. It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Narayan et al by the teaching of Rozenshein et al to include register expansions to set of existing prefix instructions as to further expand upon the goal as stated by Narayan with the use of the prefix instructions.

As per **claim 10** and in light of above rejection of claim 4, it is rejected based upon similar reasoning as the rejections of claims 7, 8, 11, and 12.

As per **claim 16** and in light of the above rejection of claim 4, it is rejected based upon similar reasoning as the rejections of claims 13, 14, 17, 18, and 19.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

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January 3, 2007

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1/5/2007